RISC & CISC Architectures

A Brief Comparison

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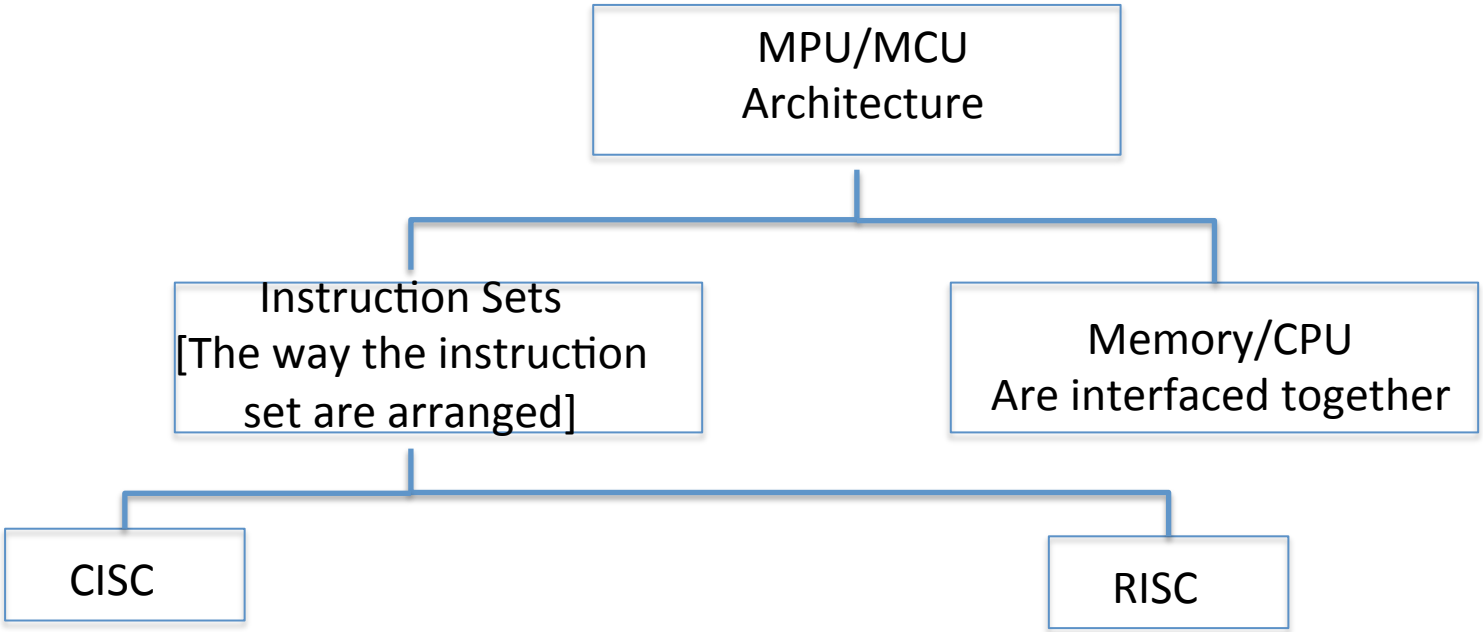


- Complex Instruction set computer
- Developed by Intel
- X86 Machines (Windows)
- The basic idea:

Instructions are

- More complex
- Fewer
- Slower

→ ALU

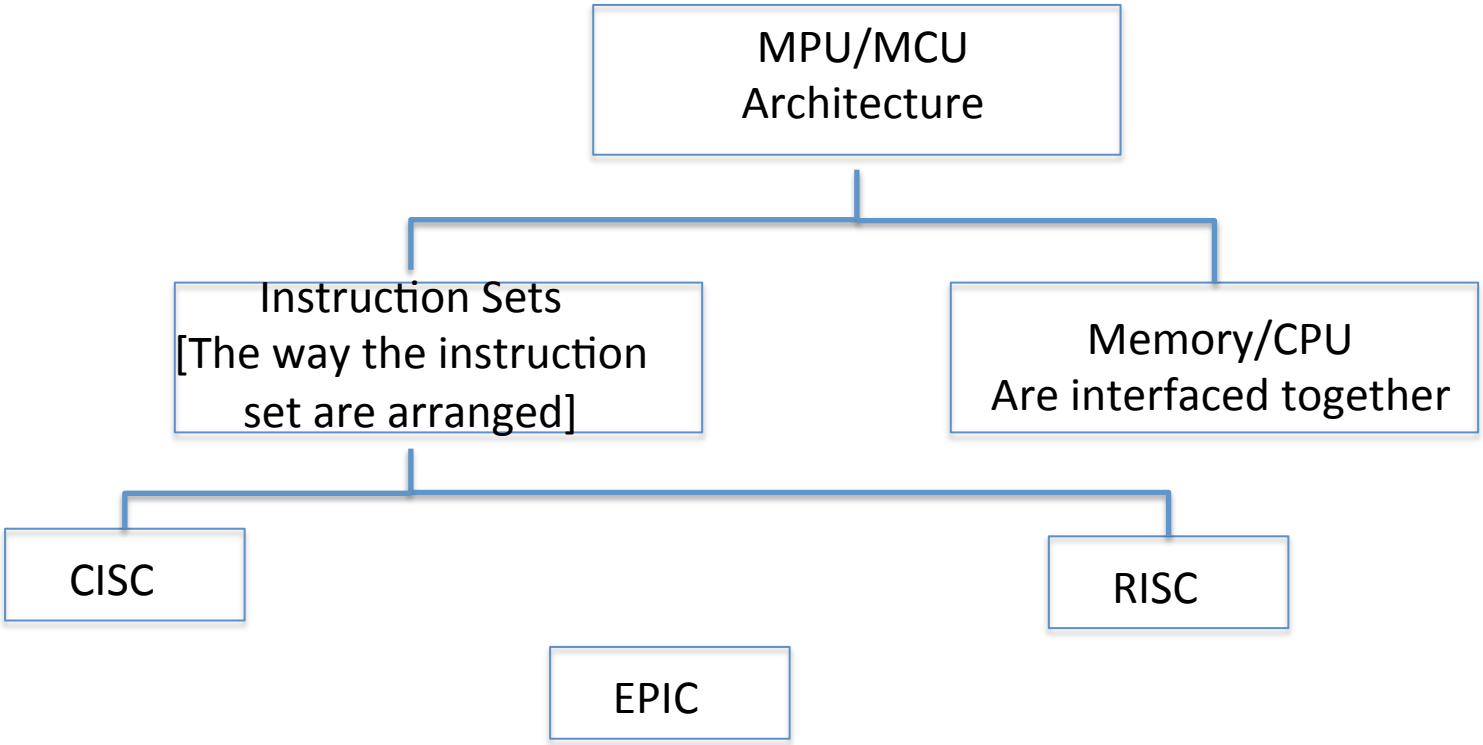
- Reduced Instruction set computer
- Evolved around 1980
- Chips by Apple / Most Cell phone
- The basic idea:

Instructions are:

- Simpler
- More
- Faster

→ ALU

Both architectures are becoming more similar!

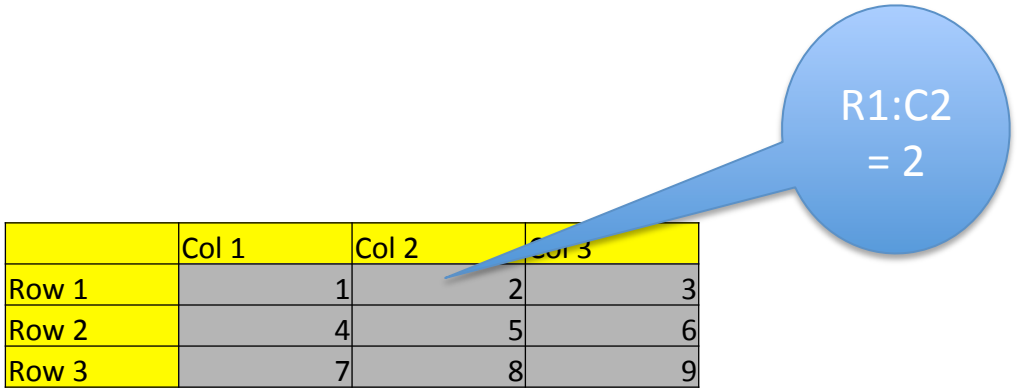


- Explicitly Parallel Instruction Computing
- Developed by Intel
- A major competitor to both RISC and CISC

Let's see an example to understand the difference more!

EXAMPLE:

Let's assume we want to write a series of codes (instructions) that multiplies two numbers from the RAM:



	Col 1	Col 2	Col 3
Row 1	1	2	3
Row 2	4	5	6
Row 3	7	8	9

CISC Instruction Set:

MULT 1:1, 2:1 ; 1 x 4 → 4 in 1:1
; (a x b = a)

RISC Instruction Set:

LOAD A, 1:1
LOAD B, 2:1
PROD A,B
STOR 1:1,A

- Simple low-level instructions (reduces instruction set)
- More lines of code!
- More RAM is utilized
- More processing

BUT→ Each instruction (code)takes only ONE CLOCK CYCLE To execute!

In general, CPU processing power in MPUs or MCUs can be measured in terms of Instructions/time (millions of instructions per second or MIPS) – when running a particular program.

Another way to look at this is to measure performance in terms of time/program:

$$\frac{\text{time}}{\text{program}} = \frac{\text{time}}{\text{cycle}} \times \frac{\text{cycles}}{\text{instruction}} \times \frac{\text{instructions}}{\text{program}}$$

RISC Focus is To minimize this!

CISC Focus is to minimize this!

Now you do the next example…..

Do this EXAMPLE

Consider the following
REGISTER content (RAM)

	Col 1	Col 2	Col 3
Row 1	1	2	3
Row 2	4	5	6
Row 3	7	8	9

CISC Instruction Set:
MULT 2:1, 3:1;
MULT 2:1, 3:2;

4x7=28→2:1

Assume each MULT instruction takes **10** - clock cycle and each clock cycle is 1 MHz (1usec).

Q1: What is the result of the above instruction sets?

Q2: What will be the equivalent RISC instruction set?

Q3: How many instruction sets will be used in RISC?

Q4: What is time/program for CISC?

Q5: What is time/program for RISC?